Amendments to the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A method of processing first header information of a reception packet to provide instruction regarding processing of second header information, the method comprising the steps of:

(a) separating error correction data, payload data and first header information from the reception packet; and

(b) processing, in one clock cycle, the first header information in a protocol processor unit to provide, by an end of the one clock cycle, selected instructions for processing second header information.

2. (Original) The method of claim 1, further comprising:

generating payload flags based on the selected instructions, wherein

the payload flags are used by execution units for processing the accompanying payload data.

3. (Original) The method of claim 1, wherein the selected instructions are stored in at least one look up table and provided based on results of processing the first header information.

4. (Original) The method of claim 1, wherein the second header information is header information immediately following the first header information.

5. (Original) The method of claim 1, wherein step (b) comprises:

separating at least one field in the first header information for processing,

wherein the processing includes one of :

comparing the at least one field to predetermined data, and

processing the at least one field in an arithmetic and logic unit;

generating control signals and flags based on results of the comparing and processing;

matching the control signals and flags to instructions

provided in a first look-up table; and

providing the selected instructions for processing the second header information based on the matched control signals and flags.

6. (Original) The method of claim 5, wherein a plurality fields are separated from the first header information, including at least a first field and a second field, where

the first field is compared to the predetermined data, and

the second field is processed in the arithmetic and logic unit.

7. (Original) The method of claim 1, wherein step (b) comprises:

separating a plurality of fields in the first header information;

comparing the plurality of fields with a plurality of parameters supplied from a second look-up table, simultaneously, using a plurality of comparators in a compare unit;

generating a match flag indicating a match between at least one of the plurality of fields and one of the plurality of parameters;

generating an address based on a result of the comparing;

matching the address to a value in a third look up table; and

using the matched value and the match flag to provide instructions for processing the second header information.

8. (Original) The method of claim 7, where the third look up table includes a plurality of individual look up tables, wherein

a first control signal provided from an instruction decoder selects one of the plurality of individual lookup tables in the third look up table, and

the address is matched to the value in the selected individual lookup table.

9. (Currently amended) The method of claim 5, wherein when the step of comparing the at least one field to the predetermined ~~value~~ data further comprises:

comparing a portion of the at least one field to the predetermined value when the at least one field is longer than a length of a comparator to generate a partial comparison result;

outputting the partial comparison result as long as a previous partial comparison result is a predetermined value; and

repeating the comparing step for each portion of the at least one field.

10. (Original) The method of claim 1, wherein margins between protocol layers of the header information are eliminated prior to processing.

11. (Currently amended) The method of claim 1, wherein the error detection data is processed in parallel simultaneously with the processing of the first header information.

12. (Original) A protocol processor for processing first header information of a reception packet to provide instructions for processing second header information,

comprising:

a buffer adapted to buffer header information separated out from the reception packet; and

a protocol processor unit adapted to process, in one clock cycle, the first header information sent from the buffer to provide, by an end of the first clock cycle, instructions regarding processing of the second header information of the reception packet.

13. (original) The protocol processor of claim 12, wherein the protocol processor comprises a payload flag generating unit to generate payload flags based on the instructions, wherein

the payload flags are used by execution units to guide processing of the accompanying payload data.

14. (Currently amended) The protocol processor of claim 12, further comprising at least one look up table in which the ~~selected~~ instructions are stored, wherein ~~the~~ selected instructions are provided based on results of ~~preccessing~~ processing of the first header information.

15. (Original) The protocol processor of claim 12, wherein the second header information is header information immediately following the first header information.

16. (Original) The protocol processor according to claim 12, wherein the protocol processor unit further comprises:

a multiple field extractor adapted to extract at least one field of the first header information, where the at least one field is passed to one of:

a compare unit adapted to compare the at least one field to a predetermined value, and

an arithmetic and logic unit adapted to process the at least one field to provide updated connection state variables which are stored in a register file and arithmetic and logic unit flags;

a program control flag generation unit adapted to generate control signals and flags based on a result from the compare unit and the flags and state variables provided by the arithmetic logic unit; and

a program and instruction decoding unit adapted to match (a) the control signals and flags generated by the

program control flag generating unit and (b) instructions in a first look up table, and to output selected instructions that match the control signals and flags, wherein the selected instructions are used in processing the second header information.

17. (Currently amended) The protocol processor of claim 16, wherein the multiple field extractor extracts a plurality of fields from the first header information including at least a first field and a second field, where

the compare unit compares the first field to the predetermined ~~data~~ value, and

the arithmetic and logic unit processes the second field to provide updated connection state variables which are stored in the register file and arithmetic and logic unit flags.

18. (Original) The protocol processor of claim 12, wherein the buffer is capable of buffering data words of different sizes and comprises:

a plurality of registers, one of the plurality of registers storing the first header information separated out

from the reception packet being processed, and other ones of the plurality of registers being used to buffer header information when necessary.

19. (Original) The protocol processor of claim 16, wherein the program and instruction decoding unit further comprises:

a next program counter calculation unit adapted to determined a next program counter value based on the control signals and flags provided by the program control flag generation unit;

a program counter adapted to receive the next program counter value provided by the next program counter calculation unit and determine a program counter value based on the next program counter value;

wherein the first lookup table matches (a) the program counter value provided by the program counter to (b) a selected instruction, and

an instruction decoder which receives the selected instruction from the first lookup table and decodes the instruction to provide decoded instructions used in decoding the second header information.

20. (Currently amended) The protocol processor according to claim ~~12~~ 16, further comprising:

a plurality of comparators adapted to perform a plurality of comparisons located in the compare unit;

a second look up table which receives a vector input and outputs a vector, parameters of which the at least one field is compared to using the plurality of comparators;

a flag to address translation unit which receives the result of the comparisons and generates a match flag indicating at least one of the plurality of parameters matches the at least one field of the first header information and an address corresponding to another flag generated based on a result of the multiple comparisons; and

a third look up table which receives the address from the flag to address translation unit which is matched to a value in a third look up table; wherein

the value matched in the third look up table and the match flag are passed to a next program counter calculation unit to provide a next program counter value which is passed to the program counter to be matched with an instruction in the first look up table to provide instructions for

processing the second header information.

21. (Original) The protocol processor of claim 20, wherein the third look up table comprises a plurality of individual look up tables and a first control signal selects one of the plurality of look up tables and the address is matched to the value in the selected look up table.

22. (Original) The protocol processor unit of claim 16, wherein the compare unit compares a portion of the at least one field to the predetermined value when the at least one field is longer than a comparator to produce a partial comparison result, outputs the partial comparison result when a previous partial comparison result is of a predetermined value, and repeats the comparing for each portion of the at least one field.

23. (Original) The protocol processor of claim 12, further comprising:

an error correction accelerator unit adapted to process error correction data in parallel with the processing of first header information in the protocol processor unit.

24. (Original) The protocol processor of claim 12, wherein margins between protocol layers in the first header information are eliminated prior to processing in the protocol processor unit.

25. (Original) A program storage medium readable by a processor, tangibly embodying a program of instructions executed by the processor to perform method steps for processing first header information of a reception packet to provide instruction regarding processing of second header information, wherein the method steps comprise:

(a) separating error correction data, payload data and header information from the reception packet; and

(b) processing, in one clock cycle, the first header information in a protocol processor unit to provide, by an end of the one clock cycle, selected instructions for decoding second header information.

26. (Original) The program storage medium of claim 25, wherein the method steps further include:

generating payload flags based on the selected

instructions, wherein

the payload flags are used by execution units to process the accompanying payload data.

27. (Currently amended) The program storage medium of claim ~~23~~ 25, wherein the selected instructions are stored in at least one look up table and are provided based on results of the processing of the first header information.

28. (Currently amended) The program storage medium of claim ~~23~~ 25, wherein the second header information is header information immediately following the first header information.